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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,874	09/27/2000	Chou H. Li		7377

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EXAMINER
MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/670,874	LI, CHOU H.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *66-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *66-95* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *28 June 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Examiner has noted that the applicant has responded to the election restriction from the last communication response. The applicant has elected the Device and cancelled existing claims and redirected to claims 66-95 for further examination without traverse. Examiner makes the restriction final.

Drawings

1. Figures 1, 2, and 3a-b should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: The disclosure describes Figure 6 to be an atomic molecular chain or sheet used in flexible 3-D atomic diode or transistor array or circuit on page 17, but the application does not contain a Figure 6 in the drawings.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 68, 71, 78, 85-86, 92, and 94-95 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Referring to claim 68, a solid-state device, in which the solid state material layer has a central portion of zero width which is symmetrical with respect to a central bisecting plane thereof whereby no weaker side exists, (Examiner is unsure what is meant by zero width).

4. Referring to claim 71, a solid-state device, in which the solid state material layer is sufficiently thin and flexible so as to yield significantly thereby preventing device failures through a curvature-related stress-relieving and strain-relieving mechanism, (Examiner is unsure what is meant by a mechanism).

5. Referring to claim 78, a solid-state device, including: a first and a second solid state material pockets positioned adjacent to, but laterally separated by a gap, on the top surface of the substrate; the solid state material layer thereby bridging the gap between the two adjacent solid state material pockets; and at least a portion of **the solid state material layer having an accuracy in thickness of no more than three atomic layers and** being uniformly bonded uniformly to at least a selected area of the substrate avoiding imperfectly bonding interfacial region, (Examiner is unsure what is meant by a the highlighted section of the claim. Is the accuracy the tolerances of the thickness and is the atomic layers one atom thick).

6. Referring to claim 85, a solid-state device, including a PN junction region having a curved adjoining surface and provided on the substrate; and at least one of inevitable thermal mismatch stress and in situ volume change strain generated during device processing being reduced but not eliminated, **through a curvature-related strain-relieving and stress-relieving mechanism** operating on the curved adjoining surface; the remaining residual strain and stress on the curved adjoining surface of the PN junction region being utilized to improve a device performance, (Examiner is unsure what is meant by a mechanism).

7. Referring to claim 86, a solid-state device, in which: the substrate is a semiconductor of one conductivity type and has a matching part contacting the curved adjoining surface of the PN junction region; at least one of the first and second solid state material pockets is a semiconductor of the opposite conductivity type thereby forming at least one PN junction region where the substrate meets the curved adjoining portion of the at least one solid state material pocket, the PN junction region is within 40 atomic layers from the substrate; **and the stresses and strains are reduced, but not completely eliminated, by a curvature-related stress-relieving mechanism; and the remaining stresses and strains still provide sufficient stresses and strains to favorably affect characteristics of the PN junction region,** (Examiner is unsure what is meant by a mechanism).

8. Referring to claim 92, a solid-state device in which the solid-state material layer is curved to minimize thermal mismatch stresses through a curvature-related strain relieving and stress-relieving mechanism, (Examiner is unsure what is meant by a mechanism).

9. Referring to claim 94, a solid-state device, further comprising: a second solid state material pocket positioned on a second selected surface of the substrate, and laterally adjacent to,

but separated by a gap from, the at least one first solid state material pocket, and in which: the solid-state material layer fills the gap between the two material pockets while contacts and metallurgically perfectly bonds uniformly with a second specified portion of the second solid state material pocket; **and the solid state material layer is mechanically perfect** and is no more than 3 to 40 Angstroms thick, (Examiner is unsure what mechanically perfect is?).

10. Referring to claim 95, a mass-produced solid state device comprising: a solid state material substrate; a left and a right adjacent solid state material pockets laterally separated by a gap and positioned on a common top surface of the substrate; a curved solid state material layer which: a) has a radius of curvature of no more than 1,0 micron; and b) is positioned an the top surface of the substrate to bridge the gap between the two solid state material pocket; and at least a portion of the solid state material layer being metallurgically continuously banded to at least a selected area of the top surface of the substrate **with a mechanically perfect bonding interfacial region to avoid imperfectly bonded material layer leading to poor device yield, performance, reproducibility, reliability, and life**, (Examiner is unsure what is meant by mechanically perfect and imperfectly bond).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 66-67, 69-70, 72-79, 81, 84-88, & 93-95 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,696,402 Li.

11. Referring to claim 66, a solid-state device comprising: a solid state material substrate having a top surface, (Figure 1 #13); a solid state material layer, (Figure 1 #11), **no more than 3 to 40 Angstroms thick, (See * below),** having at least one smooth major surface, (Figure 1 the surface of layer #11 that abuts with the top surface of the substrate #13), and positioned on the top surface of the substrate, (Figure 1 #13); at least a portion of the solid state material layer, (Figure 1 #11), **being metallurgically perfectly bonded uniformly to the at least a selected portion of the solid state device achieving thermochemical stability of a bonding interfacial region, (See ** below).**

*Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

**Initially, and with respect to claims 66-95, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

12. Referring to claim 67, a solid-state device, in which the solids state material layer, (Figure 1 #11), has at least a number of the following features: a) having an atomically smoothed bottom surface; **b) having a curved top surface, (Figure 1 #11)**; c) having an atomically liquid-smoothed gate bottom layer; c) made of purified material; d) made of strengthened material; e) accurate to one atomic layer in thickness; f) aged by liquid diffusion; f) fine-grained or subgrained; h) oriented grains or subgrains; i) narrow grains or subgrains; and j) stronger than unbonded material; the number being selected from the group consisting of one, two, and three.

13. Referring to claim 69, a solid-state device, in which the solid state material layer is formed using real-time monitoring and closed-loop feedback control to achieve a precision of one to several atoms on a material layer dimension selected from the group consisting of thickness, depth, curvature, shape, size, chemical composition profiling, and lateral location, **(See ** below).**

14. Referring to claim 70, a solid-state device, in which at least a portion of the solid state material layer is bonded to the substrate with an initially liquid bonding material; the liquid bonding material wetting and filling surface defects on the solid state material layer and then solidifying and converting these liquid-filled surface defects into solid reinforcements, whereby the bonded material layer is stronger than the unbonded solid state material itself, **(See ** below).**

15. Referring to claim 72, a solid-state device, in which the solid state material layer is formed at least partly by laser heating to melt the solid state material layer; and including a controllably solidifying the melted layer material into a liquid-diffusion aged, solid state material layer, **(See ** below).**

16. Referring to claim 73, a solid-state device, having a thickness of less than a micron to one atomic layer thereby forming a thin-film integrated circuit device, **(See * below).**

*Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

17. Referring to claim 74, a solid-state device, wherein the solid-state material layer, (Figure 1 #11), is curved, (Figure 1 #18), with a radius of curvature of less than a value selected from the group consisting of 0.5 microns and I micron, (Col. 5 Line 13-14).

18. Referring to claim 75, a solid-state device, in which the solid state material layer is made by a melting and solidification process; the purity of material of the layer being improved due to the melting and solidification by at least one order of magnitude based on a segregation coefficient according to a relevant alloy phase diagram, **(See ** below).**

19. Referring to claim 76, a solid-state device, in which the solid state material layer has at least one atomically smooth major surface produced by an atomic smoothing process, **(See ** below).**

20. Referring to claim 77, a solid-state device, in which the solid-state material layer is made by ion implantation under 1 kilovolt of implanting voltage to achieve a depth accurate to atomic layers, **(See ** below).**

21. Referring to claim 78, a solid-state device, including: a first and a second solid state material pockets, (Figure 3a #33 & **See *** below**), positioned adjacent to, but laterally separated by a gap, on the top surface of the substrate, (Figure 3a #36); the solid state material

layer, (Figure 3a #31), thereby bridging the gap between the two adjacent solid state material pockets, (Figure 3a #33); and **at least a portion of the solid state material layer having an accuracy in thickness of no more than three atomic layers, (112 rejection see above),** *and* **being uniformly bonded uniformly to at least a selected area of the substrate avoiding imperfectly bonding interfacial region, (See ** below).**

*** U.S. Patent No. 5,696,402 Li. discloses the claimed invention except for first and second solid-state material pockets. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a first and second solid-state material pockets, since it has been held that mere duplication of the essential working parts of a device involve only routine skill in the art. St. Regis Paper Co. vs. Bemis Co. 193USPQ8

22. Referring to claim 79, a solid-state device, in which: at least a part of the substrate is a semiconductor of a first conductivity type, (Figure 3a #36 p-type); and at least one of the semiconductor pockets is of a second conductivity type, (Figure 3a #33 n-type), forming at least one PN junction region where the part of the substrate, (Figure 3a #36) contacts the at least one semiconductor material pocket, (Figure 3a #33).

23. Referring to claim 81, a solid-state device, in which the substrate material is selected from the group consisting of Si, Ge, SI-GO, InP, InSb, GaAs, SiC, InAs, superconductor, diamond, semiconductor material, intrinsic semiconductor material, substantially electrically insulating material, and substantially electrically conducting material, and mixture thereof, (Col. 4 Lines 24-29).

24. Referring to claim 84, a solid-state device, in which at least a major portion of the substrate, (Figure 3a #36), solid-state material pockets, (Figure 3a #35), solid state material layer,

and electrical contacts are selected to consist essentially of a single intrinsic doped, (the substrate and the pocket material are both p and n type dopants and not n+ or p+,) and less doped semiconductor material **whereby the device is made resistant to dynamic forces due to impacts, vibrations, and large and rapid accelerations and decelerations, because the plurality of the selected device component materials have practically the same density and differ from each other by only ppm or ppb of impurities, (See ** below).**

25. Referring to claim 85, a solid-state device, including a PN junction region having a curved adjoining surface, (Figure 3a), and provided on the substrate, (Figure 3a # 36); **and at least one of inevitable thermal mismatch stress and in situ volume change strain generated during device processing being reduced but not eliminated, (See ** below), through a curvature-related strain-relieving and stress-relieving mechanism, (112 rejection see above), operating on the curved adjoining surface; the remaining residual strain and stress on the curved adjoining surface of the PN junction region being utilized to improve a device performance, (See ** below).**

26. Referring to claim 86, a solid-state device, in which: the substrate is a semiconductor of one conductivity type, (Figure 3a #36 p-type), and has a matching part contacting the curved adjoining surface of the PN junction region, (Figure 3a #36 and #35); at least one of the first and second solid state material pockets, (Figure 3a #33 & See *** below), is a semiconductor of the opposite conductivity type, (Figure 3a #35 n-type), thereby forming at least one PN junction region, (Figure 3a #36 and #35), where the substrate, (Figure 3a #36), meets the curved adjoining portion of the at least one solid state material pocket, (Figure 3a #33), the PN junction region, (Figure 3a #36 and #35), is **within 40 atomic layers, (See **** below),** from the substrate; **and**

the stresses and strains are reduced, but not completely eliminated, by a curvature-related stress-relieving mechanism; and the remaining stresses and strains still provide sufficient stresses and strains to favorably affect characteristics of the PN junction region, (See 112 rejection above).

*** U.S. Patent No. 5,696,402 Li. discloses the claimed invention except for first and second solid-state material pockets. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a first and second solid-state material pockets, since it has been held that mere duplication of the essential working parts of a device involve only routine skill in the art. St. Regis Paper Co. vs. Bemis Co. 193USPQ8

27. Referring to claim 87, a solid-state device, in which the solid state material layer has been superficially ion-implanted with dopants in high concentrations therein-, the superficially ion-implanted layer being rapidly laser spike melted to have superficial liquidisation and a very shallow, highly activated doped region due to the high spike heating rates allowing much greater dopant concentrations than the thermal equilibrium phase-diagram values, **(See ** below).**

28. Referring to claim 88, a solid-state device, in which the solid state material layer is an electrically insulating, (Figure 3a # 31 Col. 15 Line 38-39), wavy and curved field layer **formed by at least partly ion implanting with an ion-implanting beam into, (See ** below),** a silicon material substrate, (Col. 4 Lines 24-29), **a substance selected from the group consisting of oxygen and nitrogen; at least one of the substrate and the ion-implanting beam having a wavy and curved movement relative to the other during the ion-implanting process to produce the wavy and curved field layer, (See ** below).**

29. Referring to claim 93, a mass-produced solid state device comprising: a solid state material substrate, (Figure 3a #36); at least one first solid state material pocket, (Figure 3a #33), positioned on a first selected surface of the substrate, (Figure 3a #36); and a solid state material layer, (Figure 3a #31), having at least one atomically smooth major surface, (Figure 3a the surface of layer #31 that abuts with the top surface of the substrate #36), which contacts **and metallurgically perfectly bonds uniformly, (See ** below),** the first selected surface of the substrate, (Figure 3a #36); to a first specified portion of the at least one first solid state material pocket, (Figure 3a #33).

30. Referring to claim 94, a solid-state device, further comprising: a second solid state material pocket, (Figure 3a #33 & **See *** below**), positioned on a second selected surface of the substrate, (Figure 3a #36), and laterally adjacent to, but separated by a gap from, the at least one first solid state material pocket, (Figure 3a #33), and in which: the solid-state material layer, (Figure 3a #31), fills the gap between the two material pockets, (Figure 3a #33 & **See *** below**), while contacts **and metallurgically perfectly bonds uniformly, (See** below),** with a second specified portion of the second solid state material pocket, (Figure 3a #33 & **See *** below**), and the solid state material layer, (Figure 3a #31), **is mechanically perfect, (See 112 rejection above), and is no more than 3 to 40 Angstroms thick, (See * below).**

*Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

*** U.S. Patent No. 5,696,402 Li. discloses the claimed invention except for first and second solid-state material pockets. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a first and second solid-state material pockets, since it has been held that mere duplication of the essential working parts of a device involve only routine skill in the art. St. Regis Paper Co. vs. Bemis Co. 193USPQ8

31. Referring to claim 95, a mass-produced solid state device comprising: a solid state material substrate, (Figure 3a #13); a left and a right adjacent solid state material pockets, (Figure 3a #19 & **See *** below**), laterally separated by a gap and positioned on a common top surface of the substrate, (Figure 3a #13); a curved solid state material layer, (Figure 3a #11), which: a) has a radius of curvature of no more than 1.0 micron, (Col. 5 Line 13-14); and b) is positioned an the top surface of the substrate, (Figure 3a #13), to bridge the gap between the two solid state material pocket, (Figure 3a #19 & **See *** below**); and at least a portion of the solid state material layer, (Figure 3a #11), **being metallurgically continuously banded, (See ** below),** to at least a selected area of the top surface of the substrate, (Figure 3a #13), **with a mechanically perfect bonding interfacial region to avoid imperfectly bonded material layer leading to poor device yield, performance, reproducibility, reliability, and life, (See 112 rejection above).**

**Initially, and with respect to claims 66-95, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ

90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

Claim Rejections - 35 USC § 103

Claims 66, 80, 82-83, and 89-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,371,406 Li.

32. Referring to claim 66, a solid-state device comprising: a solid state material substrate having a top surface, (Figure 18 #1); a solid state material layer, (Figure 18 #2), **no more than 3 to 40 Angstroms thick, (See * below),** having at least one smooth major surface, (Figure 18 the surface of layer #2 that abuts with the top surface of the substrate #1), and positioned on the top surface of the substrate, (Figure 18 #1); at least a portion of the solid state material layer, (Figure 18 #2), **being metallurgically perfectly bonded uniformly to the at least a selected portion of the solid state device achieving thermochemical stability of a bonding interfacial region, (See ** below).**

*Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant

must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

**Initially, and with respect to claims 66-95, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

33. Referring to claim 80, a solid-state device, in which the solid-state material layer is selected from the group consisting of a gate layer, (Figure 18 #2), and a field layer, (U.S. Patent No. 4,371,406 Li. discloses the claimed invention except for the field layer. It would have been obvious to one skilled in the art at the time the invention was made to have a field layer next to the gate layer since it was known in the art that gates are insulated from each other by a field layer).

34. Referring to claim 82, a solid-state device, selected from the group consisting of metal-oxide semiconductor (MOS) device, (Col. 21 Liness 14-15), and conductor-insulator-semiconductor (CIS) device, thin-film integrated circuit, and flexible integrated circuit.

35. Referring to claim 83, a solid-state device, in which: the solid state material pockets are respectively source and drain semiconductor pockets, (Figure 18 #3), in a CMOS device, (It would have been obvious to one skilled in the art at the time the invention was made to have a implement the claimed invention into a CMOS from a MOS design since it was known in the art that CMOS chips are MOS chips); the solid state material layer is a gate layer, (Figure 18 #2),

bridging the two pockets, (Figure 18 #3); the gate layer material, (Figure 18 #2), **is laser heated and melted to smooth at least one of the top and bottom surfaces by an atomic surface-smoothing mechanism; and solidification of the molten gate layer material, sub-layer by sub-layer from the bottom surface up, purifies the gate layer material greatly reducing impurities and improving insulation most at a surface contacting the substrate, (See ** below).**

36. Referring to claim 89, a solid-state device, in which: the solid state material pockets are respectively source and drain semiconductor pockets, (Figure 18 #3), in a CMOS device, (It would have been obvious to one skilled in the art at the time the invention was made to have a implement the claimed invention into a CMOS from a MOS design since it was known in the art that CMOS chips are MOS chips); and the solid state material layer is a gate layer, (Figure 18 #2), bridging the gap between the two pockets, (Figure 18 #3); and including a conductive gate electrode, (Figure 18 #2 & , (It would have been obvious to one skilled in the art at the time the invention was made to have a conductive gate electrode connected to the gate to allow charges to flow), formed of an electrically conducting material and generally centered on the gate layer, (Figure 18 #2 & , (It would have been obvious to one skilled in the art at the time the invention was made to have to have the electrode made of a conductive material which allows charges to flow and centering the electrode and centering the electrode on the gate layer is the optimal position because the path has the least amount of resistance), to control flow of electronic carriers from the source to the drain, (Figure 18 #3).

37. Referring to claim 90, a solid-state device, in which- a laser heating beam melts the gate layer material and smooths at least one of top and bottom major surfaces by an atomic surface-

smoothing mechanism achieving maximum smoothness, and solidification of the molten gate layer material, sub-layer by sub-layer from the bottom surface up, purifies the gate layer material greatly reducing impurities and improving insulation most at the bottom surface facing the substrate, **(See ** below).**

38. Referring to claim 91, a solid-state device, in which: the solid state material layer is a field layer separating and electrically isolating device components from each other; the field layer on a horizontal cross-section thereof has a plurality of curved sections; and each curved section has an arc length defined by: I = r x A where I is the arc length, r is the radius of curvature of the are, and A is the subtended arc angle; each arc section being capable of flexing whereby the arc length is changed by delta I = r x delta A + A x delta r; and the changes in delta I, delta r, and delta A all being in directions to reduce thermal mismatch strain and automatically stopping when the residual mismatch strain is reduced by the changing arc length to a point such that the multiply curved field layer can tolerate without failure the residual thermal mismatch strain, **(See ** below).**

**Initially, and with respect to claims 66-95, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
September 8, 2002

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